

APPENDIX

Claims 1 and 7 now read as follows:

1. A semiconductor device comprising:

a semiconductor chip,

*B1* a protective insulating layer comprising a coating layer covering the surface of the semiconductor chip;

a plurality of connecting conductors connected to the surface of the semiconductor chip

and penetrating the coating layer beyond the outside surface of the coating layer;

wherein the connecting conductor includes a plurality of layers formed of same material

and at least one of the layers is formed as a stress-absorbing layer having lower hardness than other layer.

7. A semiconductor device comprising:

a semiconductor chip,

a protective insulating layer comprising a coating layer covering the surface of the

*B2* semiconductor chip;

a plurality of connecting conductors connected to the surface of the semiconductor chip

and penetrating the coating layer beyond the outside surface of the coating layer;

wherein the connecting conductor includes a plurality of layers formed of different

material and at least one of the layers is formed as a stress-absorbing layer having lower hardness

than other layer.

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